APPEAL NO:

In Re Application of:

Lee

Serial No. 10/766,646

Filed: January 27, 2004

For: SILICON CARBIDE IMPRINT STAMP

APPELLANTS' BRIEF

Wendell J. Jones
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TOPICAL INDEX

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:

Lee

Serial No.:10/766,646 Group Art Unit: 1765

Filed: January 27, 2004 Examiner: Chen, Eric Brice

For: SILICON CARBIDE IMPRINT STAMP

Honorable Commissioner of Patents and Trademarks
Alexandria, VA 22313-1450

APPELLANTS' BRIEF ON APPEAL

Sir:

Appellants herein file an Appeal Brief drafted in accordance with the provisions of 37 C.F.R. § 1.192(c) as follows:

I. REAL PARTY IN INTEREST

Appellants respectfully submit that the above-captioned application is assigned, in its entirety to Hewlett-Packard Development Company, having an address as shown below.

II. RELATED APPEALS AND INTERFERENCES

Appellants state that, upon information and belief, they are not aware of any co-pending appeal or interference which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-18 are pending in the present Application. Application Serial No. 10/766,646 (the instant application) as originally filed included claims 1-18. Claims 1-18 are on appeal and all applied rejections concerning Claims 1-18 are being appealed herein.

IV. STATUS OF AMENDMENTS

The response to the Office Action dated September 19, 2005 was considered in the Final Office Action dated February 22, 2006.

V. SUMMARY OF CLAIMED SUBJECT MATTER

A silicon carbide imprint stamp of the present invention is resistant to wear, damage, and breakage because a material comprising silicon carbide (SIC) is used as the material for the imprint stamp as opposed to the silicon (Si) material of prior imprint stamps. The harder silicon carbide material also provides for an imprint stamp that can be used for many imprinting operations and still retain consistent, repeatable, and accurate imprint patterns over multiple pressing steps.

Moreover, the silicon carbide imprint stamp has an increased service lifetime, therefore, the cost of manufacturing silicon carbide imprint stamp can be recovered because the imprint stamp can withstand many pressing cycles without wearing out, breaking or being damaged unlike imprint stamp that are made from silicon.

An embodiment of the present invention, as claimed in independent claim 1, is a method of fabricating a silicon carbide imprint stamp **10**. The method includes patterning a mold layer **25**, the patterning consisting of a single masking step, etching the mold layer **25** to form a cavity **25m** in the mold layer **25**, the cavity **25m** including a first feature size λ_L that is greater than or equal to a lithography limit, the etching step consisting of a single etch, depositing a spacer layer **27** on the mold layer **25**, the spacer layer **27** conformally covering a surface of the cavity **25m** and forming a spacer **21** in the cavity **25m** by aniosotropically etching the spacer layer **27** so that the spacer **21** is connected with a portion of the surface of the cavity **25m** and the spacer **21** partially fills the cavity **25m** so that the cavity **25m** includes a second feature size λ_F that is less than the lithography limit.

The method also includes depositing a material comprising silicon carbide in the cavity and on the spacer **21** to form a feature **12** positioned in the cavity **25m** and a foundation layer **11** connected with the feature **12** and at least a portion of the feature **12** includes the second feature size λ_F, planarizing the foundation layer **11** to form a substantially planar surface **11s**, bonding a handling substrate **15** with the foundation layer **11** by applying heat and pressure to the handling substrate **15** and the mold layer **25** until the handling substrate **15** and the foundation layer **11** form a mechanical bond with each other and extracting the silicon carbide imprint stamp **10** by releasing the feature **12** and the foundation layer **11** from the mold layer **25**. **Figure 7** illustrates an exemplary method and page 9 of the specification describes these features.

A second embodiment of the present invention, as claimed in

independent claim 10, is a method of fabricating a silicon carbide imprint stamp **10**. The method includes patterning a mold layer **25**, the patterning consisting of a single masking step, etching the mold layer **25** to form a cavity **25m** in the mold layer **25**, the cavity **25m** including a first feature size λ_L that is greater than or equal to a lithography limit, the etching step consisting of a single etch, depositing a spacer layer **27** on the mold layer **25**, the spacer layer **27** conformally covering a surface of the cavity **25m** and forming a spacer **21** in the cavity **25m** by aniosotropically etching the spacer layer **27** so that the spacer **21** is connected with a portion of the surface of the cavity **25m** and the spacer **21** partially fills the cavity **25m** so that the cavity **25m** includes a second feature size λ_F that is less than the lithography limit.

The method also includes depositing a material comprising silicon carbide in the cavity and on the spacer **21** to form a feature **12** positioned in the cavity **25m** and a foundation layer **11** connected with the feature **12** and at least a portion of the feature **12** includes the second feature size λ_F, planarizing the foundation layer **11** to form a substantially planar surface **11s** of the foundation layer **11**, bonding a handling substrate **15** with the glue layer by applying pressure and heat to the handling substrate **15** and the mold layer **25** until the glue layer forms a mechanical bond with the foundation layer **11** and the handling substrate **15** and extracting the silicon carbide imprint stamp **10** by releasing the feature **12** and the foundation layer **11** from the mold layer **25**. **Figure 8** illustrates an exemplary method and page 10 of the specification describes these features.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection presented are:

1) Claims 1-2, 4-5, 10-11 and 13-14 stand rejected under 35 U.S.C. § 103 (a) over Mehregany et al. (US Patent No. 6,136, 243) in view of Chou (US Patent No 6,309,580) in further view of Appellant's admitted Prior Art;

2) Claims 3 and 12 stand rejected under 35 U.S.C. § 103(a) over Mehregany et al. in view of Chou, in further view of Appellant's admitted Prior Art, in further view of Wolf, *Silicon Processing for the VLSI Era*, Vol. 4, Lattice Press (2002);

3) Claims 6-7 and 15-16 stand rejected under 35 U.S.C. § 103(a) over Mehregany et al. in view of Chou, in further view of Cheng, in further view of Applicant's admitted Prior Art, in further view of Jeong et al. (US Patent No. 6,943,117);

4) Claims 8-9 and 17-18 stand rejected under 35 U.S.C. § 103(a) over Mehregany et al. in view of Chou, in further view of Cheng, in further view of Applicant's admitted Prior Art, in further view of Rossnagel et al., *Handbook of Plasma Processing*, Noyes Publications (1990).

VII. ARGUMENTS

A. Examiner's Burden

35 U.S.C. § 103

When making an obvious rejection under 35 U.S.C. § 103, a necessary condition is that the combination of the cited references must teach or suggest all claim limitations. If the cited references do not teach or suggest every element of the claimed invention, then the cited references fail to render obvious the claimed

invention, i.e. the claimed invention is distinguishable over the combination of the cited references.

Additionally, for reference structures to be properly combined and thereby render a claimed invention obvious, there must be some motivation for the combination i.e. there must be some teaching, suggestion, or incentive to make the combination claimed by the appellant. *Northern Telecom, Inc. v. Datapoint Corp.* 15 USPQ2d 1321, 1323 (CAFC 1990). ***Motivation coming from the appellant's own disclosure is not sufficient.*** Nor is it sufficient that those of ordinary skill in the art had the capability to combine the referenced structure or understood the advantages of the combination. Although an Examiner may suggest that the structure of a primary prior art reference *could* be modified in view of a secondary prior art reference to form the claimed structure, the mere fact that the prior art *could* be so modified does not make the modification obvious ***unless the prior art suggested the desirability of the modification***. *In re Newell,* 891 F.2d 899, 13 USPQ2d 1248 (CAFC 1989). (Emphasis added.)

B. Summary of the Applied Rejections

In the Final Office Action, dated February 22, 2006, claims 1-18 were rejected under 35 U.S.C. 103(a). In particular, the Examiner stated:

> **Claims 1-2, 4-5, 10-11 and 13-14 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Mehregany et al. (US Patent No. 6,136, 243) in view of Chou (US Patent No 6,309,580) in further view of Applicant's admitted Prior Art.**
>
> **Claims 3 and 12 stand rejected under 35 U.S.C. 103(e) as being unpatentable over Mehregany et al. (US Patent No. 6,136, 243) in view of Chou (US Patent No 6,309,580) in further view of Applicant's admitted Prior Art in further view of Wolf, Silicon Processing for the VLSI Era, Vol. 4, Lattice Press.**

Claims 6-7 and 15-16 stand rejected under 35 U.S.C. 103(e) as being unpatentable over Mehregany et al. (US Patent No. 6,136, 243) in view of Chou (US Patent No 6,309,580) in further view of Chang, in further view of Applicant's admitted Prior Art, in further view of Jeong et al. (US Patent No. 6,943,117).

Claims 8-9 and 17-18 stand rejected under 35 U.S.C. 103(e) as being unpatentable over Mehregany et al. (US Patent No. 6,136, 243) in view of Chou (US Patent No 6,309,580) in further view of Chang, in further view of Applicant's admitted Prior Art, in further view of Rossnagel et al., Handbook of Plasma Processing, Noyes Publications.

Appellants respectfully request that the Board reverse the Examiner's final rejection of Claims 1-18 under 35 U.S.C. § 103(a).

C. The Cited Prior Art

U.S. Patent 6,136,243 (Mehregany et al.)

The Mehregany reference discloses a method for molding high precision components that allows inexpensive, rapid fabrication of components using a process involving a silicon substrate, in which the mold pattern is created using multiple mask layers, a deep reactive ion etch process and photolithographic patterning techniques.

U.S. Patent 6,309,580 (Chou et al.)

The Chou reference relates to methods for changing the properties of surfaces by bonding coatings of molecules to surfaces to form non-continuous coatings of molecules bonded thereto. The invention is particularly advantageous for forming mold or microreplication surfaces having coatings of molecules bonded thereto, and to processes of molding and microreplication using these coatings and

surfaces. The coatings may be referred to as non-continuous coatings as the coating material does not have to bond cohesively with itself parallel to the surface which is coated, but is bonded, molecule-by-molecule, to the surface, such as grass protrudes, blade-by-blade, from the surface of the ground.

U.S. Patent Pub. No. 2002/0137331 (Chang)

This reference discloses a method of forming contact holes of reduced dimensions by using reverse-transcription process. First, a photoresist layer is formed on the substrate, wherein the photoresist layer has a plug-like structure. Then, an oxide layer is deposited on the plug-like structure. The oxide layer is etched to expose a portion of the plug-like structure. The plug-like structure is removed to forme a hole. Next, a conformal layer is deposited on the oxide layer and the hole. Finally, the conformal oxide layer is etched whereby the width of hole is smaller then original hole.

Wolf, *Silicon Processing for the VLSI Era, Vol. 4,* Lattice Press (2002)

This reference collects the hot issues on the very recent deep submicron (less than 0.18um) semiconductor process technology, such as EUV lithography, high and low k materials, CMP, and 300mm wafer. Major processing topics include thin gate oxides, self-aligned silicides, high- and low-k dielectrics, double and triple level metal interconnects, dual damascene copper interconnects, copper seed and electroplating technology, deep uv photoresists and tools, chemical-mechanical planarization, and processing issues unique to 300-mm wafers. State of the art CMOS topics including super-steep retrograde channel doping, punchthrough-

control implants, source/drain engineering, shallow trench isolation, and more are used to illustrate the integration of deep-submicron processes into manufacturing. Increasing use of Si-Ge heterojunction bipolar transistors and silicon-on-insulator is anticipated and discussed.

U.S. Patent No. 6,943,117 (Jeong et al.)

Jeong et al. discloses a UV nanoimprint lithography process for forming nanostructures on a substrate. The process includes depositing a resist on a substrate; contacting a stamp having formed thereon nanostructures at areas corresponding to where nanostructures on the substrate are to be formed to an upper surface of the resist, and applying a predetermined pressure to the stamp in a direction toward the substrate, the contacting and applying being performed at room temperature and at low pressure; irradiating ultraviolet rays onto the resist; separating the stamp from the resist; and etching an upper surface of the substrate on which the resist is deposited. The stamp is an elementwise embossed stamp that comprises at least two element stamps, and grooves formed between adjacent element stamps and having a depth that is greater than a depth of the nanostructures formed on the element stamps.

D. Claims 1-2, 4-5, 10-11 and 13-14 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Mehregany et al. (US Patent No. 6,136, 243) in view of Chou (US Patent No 6,309,580) in further view of Applicant's admitted Prior Art.

For ease of review, Appellant reproduces independent claims 1 and 10:

1. A method of fabricating a silicon carbide imprint stamp, comprising:

patterning a mold layer, the patterning consisting of a single masking step;

etching the mold layer to form a cavity in the mold layer, the cavity including a first feature size that is greater than or equal to a lithography limit, the etching consisting of a single etch step;

depositing a spacer layer on the mold layer, the spacer layer conformally covering a surface of the cavity;

forming a spacer in the cavity by anisotropically etching the spacer layer so that the spacer is connected with a portion of the surface of the cavity and the spacer partially fills the cavity so that the cavity includes a second feature size that is less than the lithography limit;

depositing a material comprising silicon carbide in the cavity and on the spacer to form a feature positioned in the cavity and a foundation layer connected with the feature and at least a portion of the feature includes the second feature size;

planarizing the foundation layer to form a substantially planar surface;

bonding a handling substrate with the foundation layer by applying heat and pressure to the handling substrate and the mold layer until the handling substrate and the foundation layer form a mechanical bond with each other; and

extracting the silicon carbide imprint stamp by releasing the feature and the foundation layer from the mold layer.

10. A method of fabricating a silicon carbide imprint stamp, comprising:

patterning a mold layer, the patterning consisting of a single masking step;

etching the mold layer to form a cavity in the mold layer, the cavity including a first feature size that is greater than or equal to a lithography limit, the etching consisting of a single etch step;

depositing a spacer layer on the mold layer, the spacer layer conformally covering a surface of the cavity;

forming a spacer in the cavity by anisotropically etching the spacer layer so that the spacer is connected with a portion of the surface of the cavity and the spacer partially fills the cavity so that the cavity includes a second feature size that is less than the lithography limit;

depositing a material comprising silicon carbide in the cavity and on the spacer to form a feature positioned in the cavity and a foundation layer connected with the feature and at least a portion of the feature includes the second feature size;

planarizing the foundation layer to form a substantially planar surface;

depositing a glue layer on the substantially planar surface of the foundation layer;

bonding a handling substrate with the glue layer by applying pressure and heat to the handling substrate and the mold layer until the glue layer forms a mechanical bond with the foundation layer and the handling substrate; and

extracting the silicon carbide imprint stamp by releasing the feature and the foundation layer from the mold layer.

A prima facie case of obviousness under **35 U.S.C. §103(a)** requires that all claim limitations be taught or suggested by the cited prior art references and there must be a teaching, a suggestion, or a motivation to combine or modify the references to arrive at the claimed invention.

The Appellant respectfully traverses the rejections because all of the method steps of independent **Claims 1** and **10** are not taught or suggested by U.S. Patent **6,136,243** to *Mehergany*, U.S. Patent **6,309,580** to *Chou*, Published U.S. Application **2002/0137331** to *Chang*, or by the prior art disclosed in **FIGS. 1A – 5B** of the present application when those references are considered individually or in any combination.

First, *Mehergany* teaches away from patterning a mold layer and "*the patterning consisting of a single masking step*". Second, *Mehergany* also teaches away from etching the mold layer to form a cavity in the mold layer and "*the etching consisting of a single etch step*". For example, see steps (a), (b), (c), and (e) in claims 3, 5, 6, 7, and 8 in cols. 7 – 9 and claim 1 in col. 7 of *Mehergany* where: (a) is depositing and patterning of a first mask layer; (b) is depositing and patterning of a second mask layer; (c) is performing a first etch process; and (e) is performing a second etch process.

The two patterning and the two etching processes are necessary to form the shallow and deep portions of the final mold pattern in which the SiC atomizer is to be formed. See *Mehergany* figs. 1(a) – 1(f), col. 1, lines 9 – 16, and the Abstract. Not only does *Mehergany* teach away from using a single masking step and a single etch step, *Mehergany* is also silent as to dispensing with the second patterning step and the second etching step because they are necessary to form the next deepest part of the mold (see col. 4, lines 1 – 20).

The Examiner responds to this argument in the Final Office Action dated February 22, 2006 by stating "case law has held that the omission of an element and its function is obvious if the function of the element is not desired...thus, if etching to a single depth is desired, the steps of patterning consisting of a single masking step; and the etching consisting of a single etching step are obvious." Appellant asserts that the Examiner's contention is erroneous.

According to the Examiner's cited case law, omission of an element and its function is obvious ***if the function of the element if not desired***. Appellant contends that the steps of patterning with a single masking step and etching with a single etching step are desirable to reduce the overall number of steps in the manufacturing process. Accordingly since these functions are desirable, the

omission of these elements from *Mehergany* is not obvious according to the Examiner's cited case law.

Appellant further contends that the high precision part formed by the casting process of *Mehergany* is non-operative for use as an imprint stamp because the part formed using the casting process disclosed by *Mehergany* is intended for use as an actual working part of an apparatus (e.g. a fuel atomizer for turbine engines). For example, the finished atomizer in fig. 5 is not suitable as an imprint stamp because it will not produce a functional atomizer if used to emboss a media, such as photoresist, for example. The embossing would result in a negative of the atomizer being formed in the media such that orifice O would no longer be an orifice through which fluid can flow, but rather the orifice O would become a solid cylinder in the embossed media. Similarly, the raised islands I, the slots T, the annulus A, and the spin chamber would have inverse shapes that would defeat the function of the atomizer, thereby rendering the embossed part inoperative as an atomizer.

In that the atomizer of fig. 5 is made from SiC to take advantage of the superior material properties of SiC, such as resistance to erosive operating conditions, high-temperature stability, and wear resistance, for example, one skilled in the art would not be motivated to take a functional high precision SiC component and then imprint an inferior material (e.g. photoresist) with the SiC component. Even if the imprinted media is later used as the mold in a subsequent process where SiC is deposited in the mold, the resulting SiC component would not be a precise as the original functional SiC component due to replication errors induced by the imprinting process and by subsequent processing steps. Consequently, all of the process steps and their limitations as now recited in independent **Claims 1** and **10** are not taught or suggested by *Mehergany*.

The Examiner responds to this argument in the Final Office Action dated

February 22, 2006 by stating "...one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references.... *Mehergany* is a general teaching reference, which demonstrates that silicon carbide structures can be formed by depositing silicon carbide on silicon molds formed by etching...Chou teaches that imprint stamps are formed from silicon carbide using vapor desposition molding. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form an imprint stamp using *Mehergany's* method, because Chou teaches that imprint stamps are formed of silicon carbide using vapor deposition molding." Appellant respectfully disagrees.

Examiner correctly states that *Chou* discloses an imprint stamp with features 16 that can be formed from SiC. However, *Chou* is silent as to how the imprint stamp is formed. Moreover, the focus of *Chou's* disclosure is in the application of a RELEASE material 17 to the features 16 that aid in preventing a film layer 20 embossed by the stamp from adhering to the features 16 after the imprint stamp is withdrawn from the film layer 20 (see the Abstract and Fig. 1a of *Chou*). Although SiC is mentioned as one of a list of suitable materials for a release surface (see col. 6, lines 56 – 67), Chou is silent as to how one would fabricate a SiC imprint stamp. One skilled in the art would not be motivated to combine the teachings of *Chou* with those of *Chang* or *Mehergany*. First, *Chou* teaches an already formed SiC imprint stamp with feature sizes below a lithographic limit (see Figs. 2 and 3); therefore one skilled in the art would not be motivated to include the spacer teachings in the disclosure of Chang with the teachings of *Chou*. Second, as argued above, the micro-casted high resolution SiC parts as disclosed by *Mehergany* are not suitable for use as imprint stamps because imprinting with the finished SiC part merely produces a negative non-operable part in the embossed media.

As for *Chang*, in Figs. 3 - 8, the cavity 150 with reduced dimensions is formed by depositing a photoresist layer 110, followed by patterning and etching to form a plug-like structure 110 that stands proud of the substrate 100 and has a dimension W2. None of those additional steps are recited in independent **Claims 1** and **10** of the present application.

Next, the plug-like structure 110 is completely covered by a first oxide layer 120, followed by etching the first oxide layer 120 down to the plug-like structure 110 thereby exposing an upper surface of the plug-like structure 110 for a subsequent etch step were the plug-like structure 110 is removed. After removing the plug-like structure 110, the first oxide layer 120 includes a cavity 115 having a dimension W2. Next, a second oxide layer 130 is conformally deposited in the cavity, followed by an anisotropic etch step to form sidewall spacers 140a and 140b in the cavity 150.

Regarding Chang, the Examiner contends that independent **Claims 1 and 10** use the transitional phrase "comprising" whereby the transitional term "comprising", which is synonymous with "including", "containing", or "characterized by", is inclusive or open-ended and does not exclude additional, unrecited elements or method steps. Thus, Appellant's independent **Claims 1 and 10** do not exclude the several additional steps recited in the Chang reference.

However, Appellant contends that *Chang*, teaches away from the method of the present application because nothing in the claims at issue recite first forming a plug-like structure that serves as a perform around which a cavity is formed in an oxide that surrounds the a plug-like structure. The number of process steps required to execute the spacer formation disclosed by *Chang* exceeds the number of steps recited in **Claims 1** and **10**. The cited sections of *Chang* do not disclose that the steps for: forming the plug-like structure; depositing and etching the first oxide; and etching away of the plug-like structure, can be eliminated and that the conformal

deposition of the second oxide layer 130 in the cavity can occur sans the previously mentioned steps.

Therefore, one skilled in the art upon reading *Chang* would not be motivated to forego all the process steps disclosed in *Chang* and arrive at the fewer process steps for forming the spacer layer as recited in **Claims 1** and **10** of the present application.

Finally, what the Examiner contends is admitted prior art, as disclosed in **FIGS. 1A – 5B** of the present application, does not teach or suggest the deposition and etching of a spacer layer to reduce feature sizes in the mold to a sub-lithographic feature size. Moreover, the objective of the present invention was to produce a mold in which the final feature size is below the lithographic limit of the system used to pattern the mold layer. The prior art depicted in **FIGS. 1A – 5B** does not teach or suggest how to achieve that objective.

The Examiner responds to this argument in the Final Office Action dated February 22, 2006 by stating "...one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references....However, the *Chou*, *Chang* and *Mehergany* references teach or suggest the deposition and etching of a spacer layer to reduce the feature sizes in the mold to sub-lithographic feature size.

Appellant respectfully disagrees and contends that the Examiner's cited references teach away from patterning a mold layer and "*the patterning consisting of a single masking step*". The Examiner's cited references also teache away from etching the mold layer to form a cavity in the mold layer and "*the etching consisting of a single etch step*". Accordingly, all of the claim limitations as set forth in independent **Claims 1** and **10** are not taught or suggested in the cited sections of *Chou*, *Chang* and *Mehergany* considered individually or in any combination.

Consequently, **Claims 1** and **10** are non-obvious and are patentably distinct in view of *Chou*, *Chang* and *Mehergany* and the rejections of **Claims 1** and **10** under **35 U.S.C. §103(a)** ought to now be withdrawn.

Claims 2 – 9 and **11 – 18** depend from independent **Claims 1** and **10** respectively and inherit all of their limitations. Therefore, **Claims 2 – 9** and **11 – 18** are also are non-obvious and are patentably distinct in view of *Chou*, *Chang* and *Mehergany*, and the rejections of **Claims 2 – 9** and **11 – 18** under **35 U.S.C. §103(a)** ought to now be withdrawn.

E. Claims 3 and 12 stand rejected under 35 U.S.C. 103(e) as being unpatentable over Mehregany et al. (US Patent No. 6,136, 243) in view of Chou (US Patent No 6,309,580) in further view of Applicant's admitted Prior Art in further view of Wolf, Silicon Processing for the VLSI Era, Vol. 4, Lattice Press.

Insofar as the Wolf reference fails to correct the outlined deficiency of the *Chou, Mehergany* and admitted prior art references, Appellant asserts that the Examiner's proposed combination of the *Chou, Mehergany,* admitted prior art and *Wolf* references do not teach or suggest the limitations as recited in independent **Claims 1 and 10** of the present invention. Furthermore, since claims 3 and 12 are respectively dependent on independent **Claims 1 and 10**, the above-articulated arguments with regard to independent **Claims 1 and 10** apply with equal force to claims 3 and 12. Accordingly, claims 3 and 12 should be allowed over these references.

F. Claims 6-7 and 15-16 stand rejected under 35 U.S.C. 103(e) as being unpatentable over Mehregany et al. (US Patent No. 6,136, 243) in view of Chou (US Patent No 6,309,580) in further view of Chang, in further view of Applicant's admitted Prior Art, in further view of Jeong et al. (US Patent No. 6,943,117).

Again, Insofar as the *Jeong* reference fails to correct the outlined deficiency of the *Chou, Chang, Mehergany* and admitted prior art references, Appellant asserts that the Examiner's proposed combination of the *Chou, Chang, Mehergany,* admitted prior art and *Jeong* references do not teach or suggest the limitations as recited in independent **Claims 1 and 10** of the present invention. Furthermore, since claims 6-7 and 15-16 are respectively dependent on independent **Claims 1 and 10**, the above-articulated arguments with regard to independent **Claims 1 and 10** apply with equal force to claims 6-7 and 15-16. Accordingly, claims 6-7 and 15-16 should be allowed over these references.

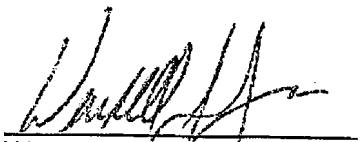
G. Claims 8-9 and 17-18 stand rejected under 35 U.S.C. 103(e) as being unpatentable over Mehregany et al. (US Patent No. 6,136, 243) in view of Chou (US Patent No 6,309,580) in further view of Chang, in further view of Applicant's admitted Prior Art, in further view of Rossnagel et al., Handbook of Plasma Processing, Noyes Publications.

Again, Insofar as the *Rossnagel* reference fails to correct the outlined deficiency of the *Chou, Chang, Mehergany* and admitted prior art references, Appellant asserts that the Examiner's proposed combination of the *Chou, Chang, Mehergany,* admitted prior art and *Rossnagel* references do not teach or suggest the limitations as recited in independent **Claims 1 and 10** of the present invention. Furthermore, since claims 8-9 and 17-18 are respectively dependent on independent **Claims 1 and 10**, the above-articulated arguments with regard to independent **Claims 1 and 10** apply with equal force to claims 8-9 and 17-18. Accordingly, claims 8-9 and 17-18 should be allowed over these references.

H. Summary of Arguments

For all the foregoing reasons, it is respectfully submitted that claims 1-18 (all the claims presently in the application) are patentable for defining subject matter which would not have been unpatentable under 35 U.S.C. § 103(a) at the time the subject matter was invented. Thus, Appellants respectfully request that the Board reverse the rejection of all the appealed claims and find each of these claims allowable. This Brief is being submitted in triplicate, and authorization for payment of the required Brief fee is contained in the cover letter for this Brief.

Very truly yours,



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VIII. CLAIMS APPENDIX

1. (Previously Amended) A method of fabricating a silicon carbide imprint stamp, comprising:

patterning a mold layer, the patterning consisting of a single masking step;

etching the mold layer to form a cavity in the mold layer, the cavity including a first feature size that is greater than or equal to a lithography limit, the etching consisting of a single etch step;

depositing a spacer layer on the mold layer, the spacer layer conformally covering a surface of the cavity;

forming a spacer in the cavity by anisotropically etching the spacer layer so that the spacer is connected with a portion of the surface of the cavity and the spacer partially fills the cavity so that the cavity includes a second feature size that is less than the lithography limit;

depositing a material comprising silicon carbide in the cavity and on the spacer to form a feature positioned in the cavity and a foundation layer connected with the feature and at least a portion of the feature includes the second feature size;

planarizing the foundation layer to form a substantially planar surface;

bonding a handling substrate with the foundation layer by applying heat and pressure to the handling substrate and the mold layer until the handling substrate and the foundation layer form a mechanical bond with each other; and

extracting the silicon carbide imprint stamp by releasing the feature and the foundation layer from the mold layer.

2. (Original) The method as set forth in Claim 1, wherein the releasing comprises a grinding a backside surface of the mold layer until the mold layer is released from the feature and the foundation layer.

3. (Original) The method as set forth in Claim 2, wherein the grinding comprises a chemical mechanical planarization process.

4. (Original) The method as set forth in Claim 2 and further comprising:

etching a remainder of the mold layer and the spacer to effectuate the releasing of the feature and the foundation layer.

5. (Original) The method as set forth in Claim 1, wherein the surface of the cavity includes a bottom surface and a sidewall surface and the spacer is connected with the sidewall surface of the cavity.

6. (Original) The method as set forth in Claim 1 and further comprising:

after the extracting, forming a master imprint stamp by mounting a plurality of the silicon carbide imprint stamps to a master substrate.

7. (Original) The method as set forth in Claim 6 and further comprising:

positioning a plurality of the silicon carbide imprint stamps in an array of rows and columns on the master substrate.

8. (Original) The method as set forth in Claim 1, wherein the forming the spacer comprises a reactive ion etching of the spacer layer.

9. (Original) The method as set forth in Claim 1, wherein the etching the mold layer comprises an anisotropic reactive ion etching of the mold layer to form the cavity.

10. (Previously Amended) A method of fabricating a silicon carbide imprint stamp, comprising:

patterning a mold layer, the patterning consisting of a single masking step ;

etching the mold layer to form a cavity in the mold layer, the cavity including a first feature size that is greater than or equal to a lithography limit , the etching consisting of a single etch step;

depositing a spacer layer on the mold layer, the spacer layer conformally covering a surface of the cavity;

forming a spacer in the cavity by anisotropically etching the spacer layer so that the spacer is connected with a portion of the surface of the cavity and the spacer partially fills the cavity so that the cavity includes a second feature size that is less than the lithography limit;

depositing a material comprising silicon carbide in the cavity and on the spacer to form a feature positioned in the cavity and a foundation layer connected with the feature and at least a portion of the feature includes the second feature size;

planarizing the foundation layer to form a substantially planar surface;

depositing a glue layer on the substantially planar surface of the foundation layer;

bonding a handling substrate with the glue layer by applying pressure and heat to the handling substrate and the mold layer until the glue layer forms a mechanical bond with the foundation layer and the handling substrate; and

extracting the silicon carbide imprint stamp by releasing the feature and the foundation layer from the mold layer.

11. (Original) The method as set forth in Claim 10, wherein the releasing comprises a grinding a backside surface of the mold layer until the mold layer is released from the feature and the foundation layer.

12. (Original) The method as set forth in Claim 11, wherein the grinding comprises a chemical mechanical planarization process.

13. (Original) The method as set forth in Claim 11 and further comprising:

etching a remainder of the mold layer and the spacer to effectuate the releasing of the feature and the foundation layer.

14. (Original) The method as set forth in Claim 10, wherein the surface of the cavity includes a bottom surface and a sidewall surface and the spacer is connected with the sidewall surface of the cavity.

15. (Original) The method as set forth in Claim 10 and further comprising:

after the extracting, forming a master imprint stamp by mounting a plurality of the silicon carbide imprint stamps to a master substrate.

16. (Original) The method as set forth in Claim 15 and further comprising:

positioning a plurality of the silicon carbide imprint stamps in an array of rows and columns on the master substrate.

17. (Original) The method as set forth in Claim 10, wherein the forming the spacer comprises a reactive ion etching of the spacer layer.

18. (Original) The method as set forth in Claim 10, wherein the etching the mold

layer comprises an anisotropic reactive ion etching of the mold layer to form the cavity.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

Appellants assert that there are no copies of decisions rendered by a court or Board to be submitted at this time.